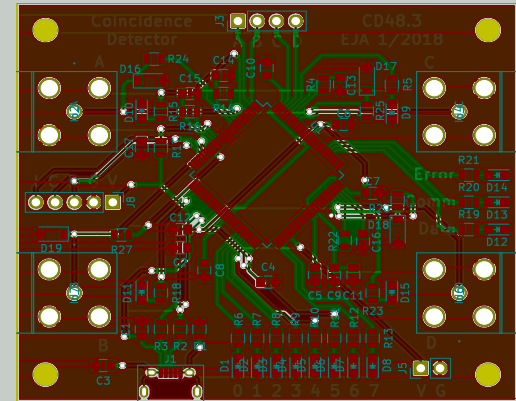# Development of a high-resolution coincidence counter using the Cypress PSoC 5LE

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⇦ Actual size

## The Problem

In quantum optics experiments, it's important to be able to detect, and count, coincidences between multiple photon detectors.

- The coincidence detector must be sensitive to the leading edges of the detection pulses.

- It should consider two pulses to be *not* coincident if the pulse leading edges occur more than 40 nanoseconds apart.

- It should be configurable, so as to watch (and count) multiple signals or combinations of signals.

- It should be able to count the pulses, and the coincidences between pulses, at rates greater than 10 kHz.

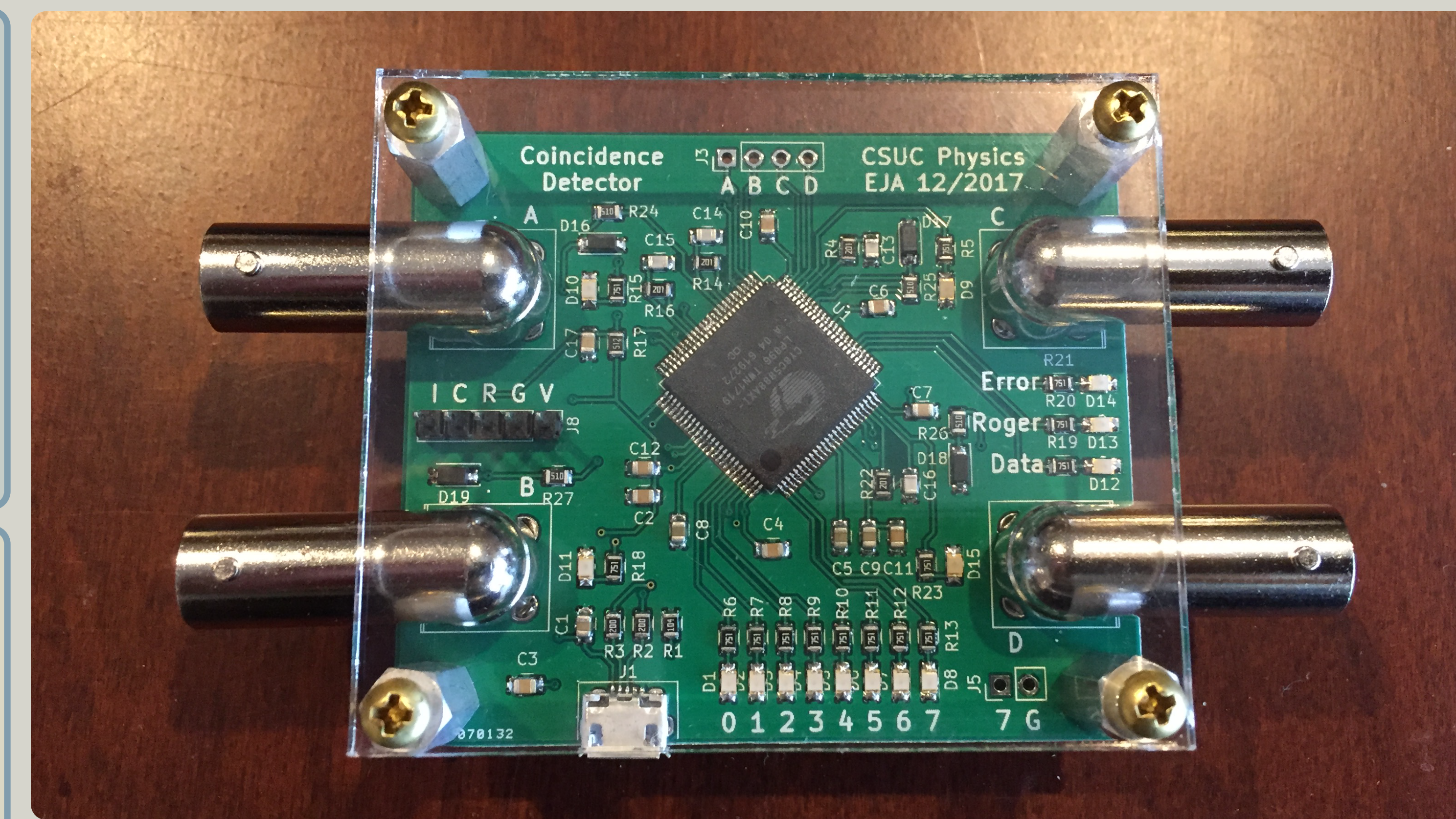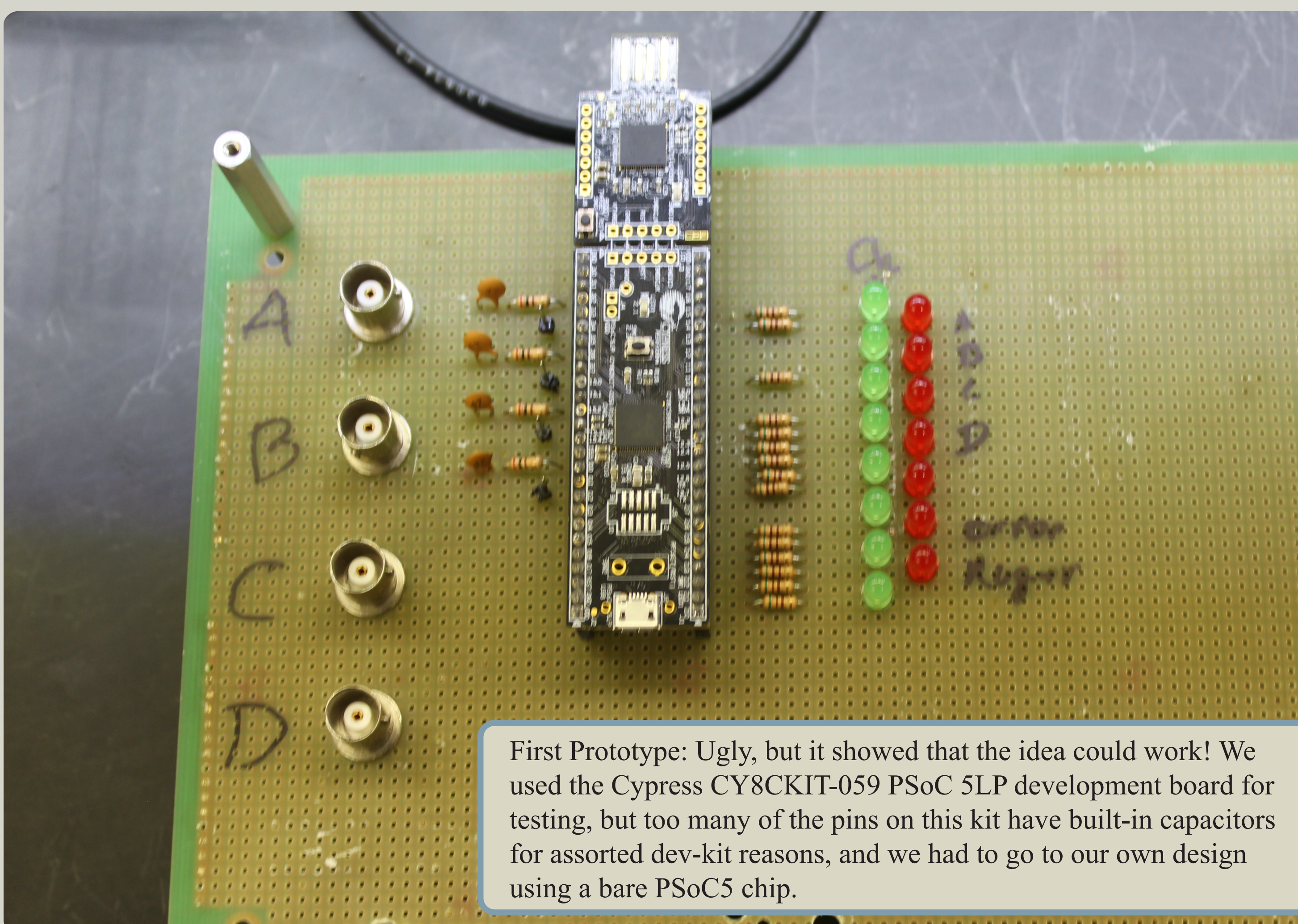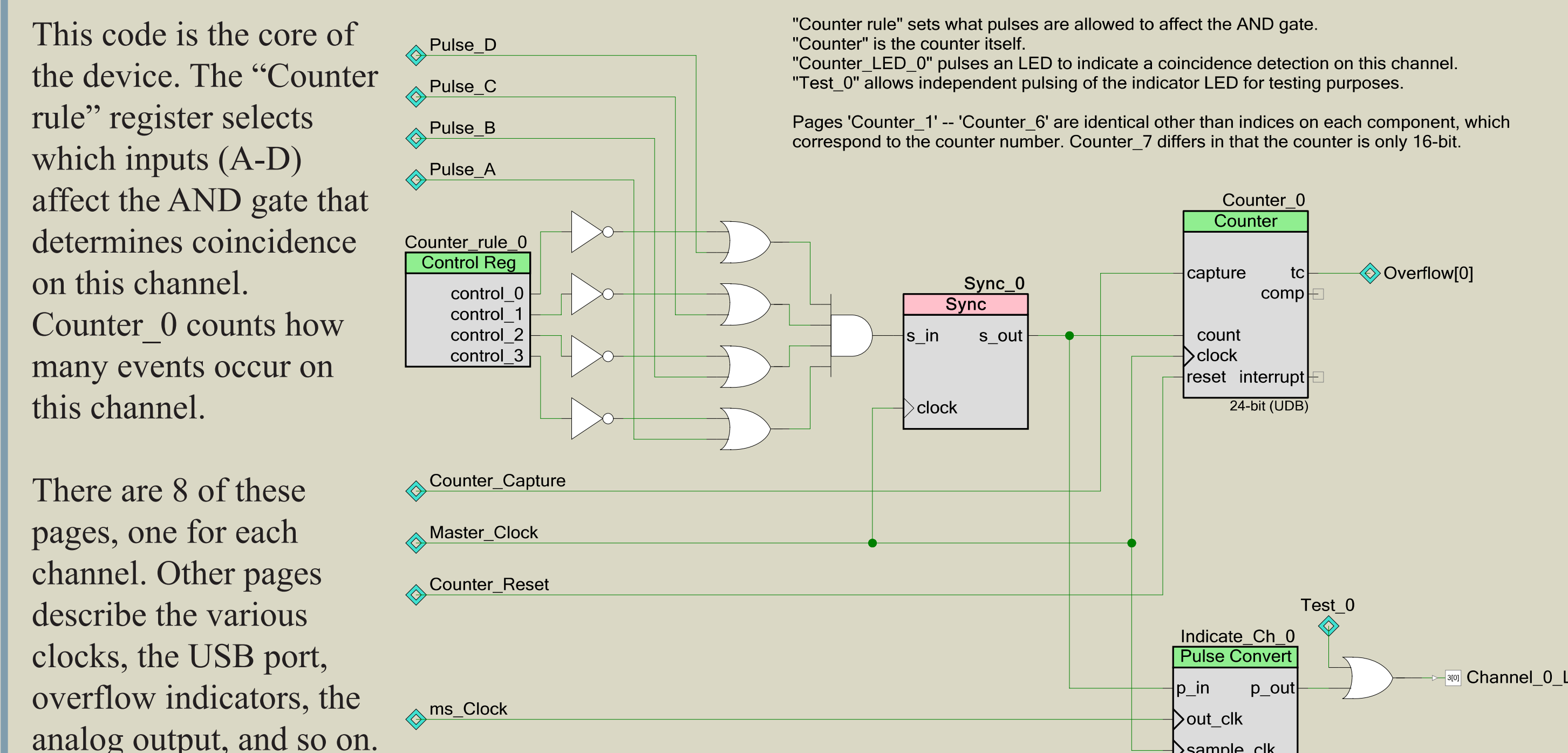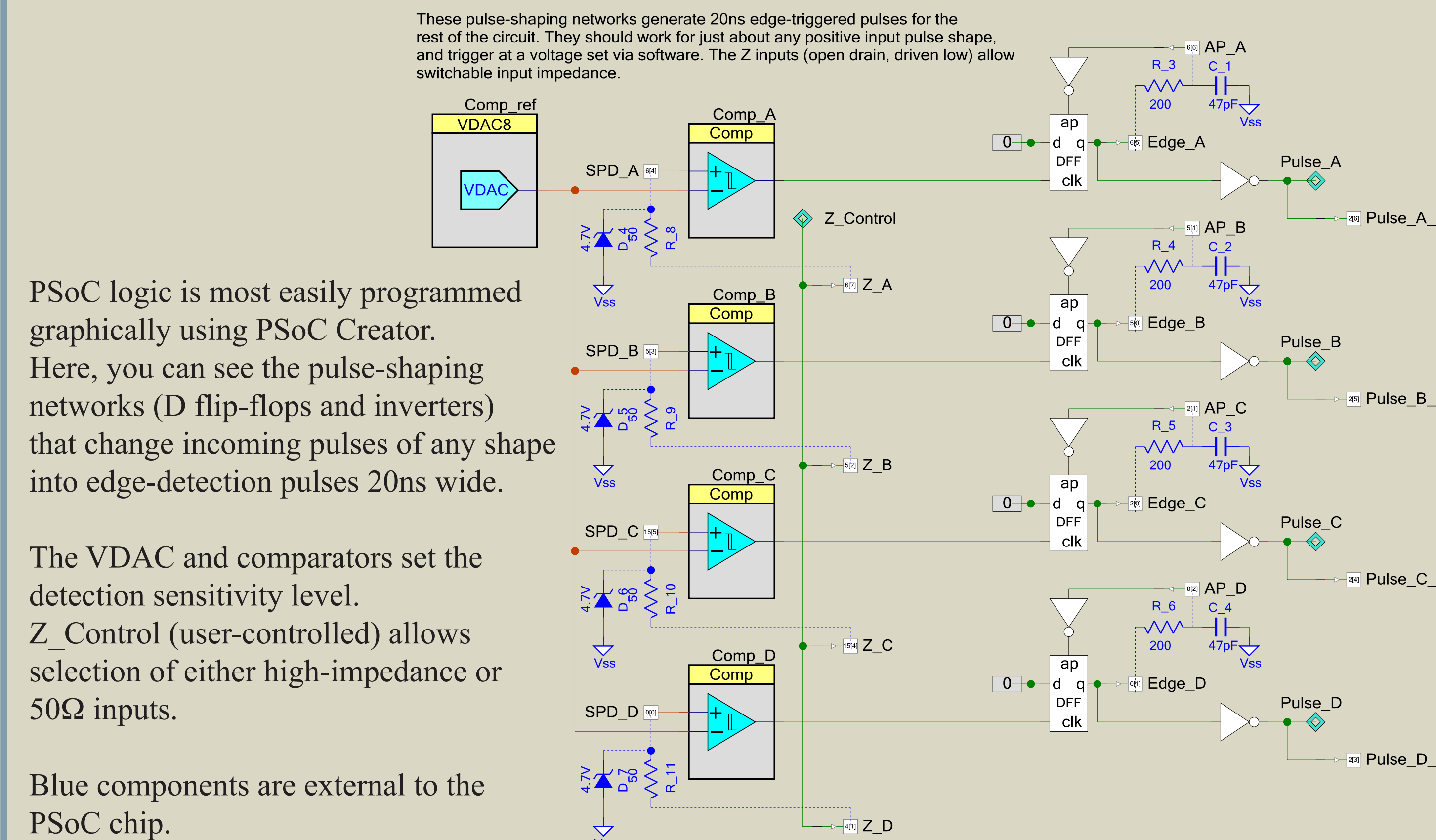- Signal discrimination capability would be a nice bonus.

## The Solution

The Programmable System on Chip offers a powerful combination of FPGA logic, configurable analog circuitry, and a Cortex M-series microprocessor. The chip can be programmed to mesh all three of these distinct capabilities into one system.

The analog circuitry provides comparators and a programmable DAC comparison level for signal discrimination. The digital logic is configured to detect edges, indicate status, and count coincidences. The microcontroller ties it all together and communicates with the operator's computer via USB.

The net result is a single-chip solution to the problem. It provides four inputs and eight count channels. Each channel can be configured to count pulses or coincident pulses on any combination of the four inputs. The control computer can set the input voltage level that qualifies as a valid pulse. The inputs can be configured to either high Z or 50-Ohm impedance. Counts can be recorded either on-demand or automatically at specified time intervals. Should the number of counts exceed the capabilities of the 24-bit counters, that's indicated as well. There is also the option of a separate computer-controlled analog output for experiment control.

As an added bonus the time sensitivity is 25ns (well below the 40ns design specification) and it can count at over 10 MHz.

PSoC logic is most easily programmed graphically using PSoC Creator. Here, you can see the pulse-shaping networks (D flip-flops and inverters) that change incoming pulses of any shape into edge-detection pulses 20ns wide.

The VDAC and comparators set the detection sensitivity level. Z_Control (user-controlled) allows selection of either high-impedance or 50Ω inputs.

Blue components are external to the PSoC chip.

This code is the core of the device. The "Counter rule" register selects which inputs (A-D) affect the AND gate that determines coincidence on this channel. Counter_0 counts how many events occur on this channel.

There are 8 of these pages, one for each channel. Other pages describe the various clocks, the USB port, overflow indicators, the analog output, and so on.



Plan A was to design a 'motherboard' that could take the CY8CKIT-059 development kit as a 'daughterboard'. The kit had extra features, though, and some of these features involved external capacitors that decreased the time resolution of pulses on those pins. Plan B required designing a surface-mount board that used a bare PSoC5 chip. After designing the board using KiCAD, we found a company that specialized in small-batch board fabrication: they provided the bare board and a solder-paste stencil. Placing the parts requires small tweezers and a steady hand, but it can be done!



Communications with the device are via USB, and it was designed with long-term cross-platform functionality in mind. All commands and responses are text-based through a virtual serial port, so any computer/language that can communicate via serial port can use it. The best software for it so far is written in LabVIEW, but it's been operated via Python, Java, and Matlab on Mac, Windows, and Linux computers.

All design files and firmware are available for non-commercial use if you wish to make your own. Commercial availability is pending, see reddogphysics.com.

First Prototype: Ugly, but it showed that the idea could work! We used the Cypress CY8CKIT-059 PSoC 5LP development board for testing, but too many of the pins on this kit have built-in capacitors for assorted dev-kit reasons, and we had to go to our own design using a bare PSoC5 chip.